Application Note

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Scalable Ethernet Service testing

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Ethernet has migrated from 1G Ethernet to 10G Ethernet to 40G Ethernet and now 100G Ethernet in just a decade, which has also brought an increase in system complexity requiring multiple FPGA and ASSP devices, High-Speed SerDes technologies, and advanced optics.

First, we have the challenges at the physical layer and moving bits at 40 or 100 Gbps speeds. Secondly, we have the challenges of scaling the upper-layer engines to deliver services and Quality of Experience (QoE) at four to ten times the current rate.

There are also challenges associated with equipping the test lab with 40G Ethernet or 100G Ethernet test ports, while maintaining compatibility with network devices capable of converting seamlessly from 10 Gbps to 40 and 100 Gbps speeds.

Physical Layer Testing

Validating 40/100G Ethernet at Layer 1 is about the basics—moving bits error free. At different sub-layers, that means different things.

Physical Medium Dependent (PMD)

Testing the PMD layer is the domain of lower-level testing instruments such as oscilloscopes, jitter stress generators, and CFP to SMA breakout cable adapters.

Physical Medium Attachment (PMA)

Testing the PMA layer involves sending pseudo-random bit sequences (PRBS), through the system and detecting errors, such as bit errors or pattern synchronization issues. The ability to test the physical pathways using unique PRBS BERT patterns reveals physical lane stability and crosstalk issues. Loopback testing is important at this level.

The architecture of the 100/40G PHY layers is shown below. The number of lanes is 20 for the 100G CAUI host interface, and 4 lanes for the 40G XLAUI interface, with the specific examples shown illustrating a 100G CAUI host interface with a LR4 100G optical device.
**Physical Layer testing (PMA)**

The increasing complexity of the Phy layer requires screening of optical devices during development and production. Use the PMA PRBS test function to determine if your 100/40 Gbps optical transceivers function correctly. Insert the transceiver optics into the Xena tester, and insert an optical loopback cable in the CFP module. Then enable PRBS for all lanes, and let the test run for at least 24 hours before verifying that there are no PRBS errors detected. The loopback cable must be clean and able to pass error-free traffic on any other known good transceiver.

- Figur 2 PHY (PCS and PMA) for 100G CAUI with LR4 optical transceiver

- Figur 3 Enable PMA PRBS per lane Tx

- Figur 4 Verify PMA PRBS per lane error statistics

Repeat this test for all optics. By measuring potential errors over a long duration, this test determines whether the optics function correctly.
To determine correctly whether the PMA layer on the DUT functions without bit errors, put the DUT in a PMA loopback (PCS loopback does not work) and then enable PRBS for all lanes on the Xena tester, and let the test run for at least 24 hours before verifying that there are no PRBS errors detected. The primary function of the PMA is to multiplex input lanes to output lanes, but this test also verifies clocking and clock recovery mechanisms in the DUT.

**Physical Coding Sub-layer (PCS)**

Testing the PCS layer involves introducing lane swapping and lane skew. Measuring the ability of the DUT to manage the virtual lane to physical SerDes lane translation is critical because lane swapping errors can lead to interface link-down problems that are difficult to debug in deployed systems.

First, configure the Xena tester to transmit L2/3 traffic from the tester to be sent across the DUT and back to the same tester port. Then, verify that header lock and alignment lock works on all Rx lanes, to verify that all lanes are recognized and are aligned. Then swap lanes randomly and verify the new Rx lane mapping. Any alignment lock issues indicate that the DUT PCS layer is not inserting the lane markers properly, and incorrect RX lane mapping indicates an issue with how the DUT transmits frames. Note that L2/3 traffic loss can be expected when the lane mapping is changed, and also when the Tx skew is changed.

To validate skew tolerance and compensation algorithms, insert a skew of 10 ns on multiple lanes and verify that the PCS markers remain aligned. Then, increase the skew until lane alignment lock is lost to find the maximum skew for the DUT. On the receive port, the amount of skew present after compensation by the system under test is reported. The Rx skew is measured with a resolution of 66 bits, which is equivalent to the size of one PCS codeword. Skew testing compares the ability of the system under test to support the standard, or report the degree to which it doesn’t match the specification.
The IEEE 802.3ba specification suggests a max PCS skew tolerance of 180 ns. The IEEE defined skew tolerances are shown below.

- Figure 7 Insert skew on random selected lanes on the Tx PCS
- Figure 8 Verify the skew insertion on Rx PCS

- Figure 9 IEEE 802.3ba defined skew tolerances

Note that for 40GBASE-R, 1 UI is equal to 97 ps at PCS lane signaling rate of 10.3125 Gbps
Note that for 100GBASE-R, 1 UI is equal to 194 ps at PCS lane signaling rate of 5.15625 Gbps

**Media Access Control (MAC)**

The Layer 2 MAC layer has similar testing issues to Layer 1. Testing the MAC layer involves measuring the ability to transmit and receive frames and handle frame check sequence (FCS) errors at all possible rates, frame lengths, and frame inter-frame gaps. The test system also introduces FCS errors, as well as counting FCS errors received.
Benchmark testing with RFC 2544 and RFC 2889

To provide a standard way of measuring and evaluating a solution, the industry has created a series of benchmarks. These benchmarks establish a uniform procedure for the generation of traffic to and from the system under test with a normalized procedure of analysis and reporting.

The ubiquitous RFC 2544 is used to verify forwarding performance and includes throughput (performance availability), back-to-back (link burstability), latency (transmission delay) and frame loss (service integrity) measurements. The Xena testers can perform the RFC 2544 test suite for 100G and 40G Ethernet interfaces at all frame sizes and at full-line rate, allowing service providers to certify that the circuit is efficient and error-free at 100% utilization at Layer 2 (VLAN) or layer 3 (IP).

Several vendors are now offering 40 Gbps enabled layer 2 switches. The RFC 2889 test suite is ideally suited for validating the performance of such switching devices, by testing at full line-rate, large-scale full-mesh test beds, and characterizing the switch’s ability to meet the demand for the low-latency and throughput performance for lossless data center Ethernet transmission.

With multicast traffic growing in importance in cloud networking applications, the RFC 2889 benchmark tests can also be used to characterize multicast-only throughput test cases where latency and throughput are key performance parameters.

Testing Multi-rate Network Ports

New commercially available Layer 2 and layer 3 network devices offer a smooth network upgrade path, by providing full flexibility to configure network ports as either 4 x 10 Gbps, or 1 x 40 Gbps. This powerful capability allows the customers to deploy 10 Gigabit Ethernet to meet current needs and be ready to transition to 40 Gigabit Ethernet without any disruption. Such devices include the Cisco Catalyst 6500 series, Juniper’s Nexus 7000 switches, as well as several others commercially available solutions.

The Xena 40 Gbps and 100 Gbps testers are the only commercially available Ethernet testers offering tri-speed test ports. Xena’s CFP based testers can support 100 Gbps, 40 Gbps, and 10 Gbps port speeds. A summary of the port speeds supported by the 100/40G Xena testers is shown in Table 1.

<table>
<thead>
<tr>
<th>Xena tester P/N</th>
<th>100 Gbps Interfaces</th>
<th>40 Gbps Interfaces</th>
<th>10 Gbps Interfaces</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1CFP100</td>
<td>1 x 100GBASE-LR4/ER4</td>
<td>1 x 40GBASE-LR4</td>
<td>4x10GBASE-LR</td>
</tr>
</tbody>
</table>
Table 1: Port speeds supported by Xena’s CFP based testers

<table>
<thead>
<tr>
<th>CFP Cage</th>
<th>1 x 100GBASE-SR10</th>
<th>2 x 40GBASE-SR4</th>
<th>8x10GBASE-SR</th>
</tr>
</thead>
<tbody>
<tr>
<td>M2CFP40</td>
<td></td>
<td>1 x 40GBASE-LR4</td>
<td>4x10GBASE-LR</td>
</tr>
<tr>
<td>(1 CFP cage)</td>
<td>2 x 40GBASE-SR4</td>
<td>8x10GBASE-SR</td>
<td></td>
</tr>
</tbody>
</table>

To change the port speed, the user must simply configure the port speed and change the physical configuration of the CFP transceiver and optical cables.

Properties | Streams | Statistics | Filters | Capture | Histograms | 40/100G | BERT | Global |
---|---|---|---|---|---|---|---|---|
Reserved by: Lab Release Module model: M2CFP40 Module serial number: 1409179 Module version number: 1.44 Upgrade Ports: 10
Time source: Free-running time
CFP status: Flexible Module temperature: N/A degrees celsius
CFP configuration: 1 x 100G 4 x 10G 2 x 40G 9 x 10G 1 x 40G

Figure 11: Select 1 x 100 Gbps CFP test module configuration in XenaManager

The unique flexibility of the Xena testers is not only useful for scaling your test lab test infrastructure from 10 Gbps, to 40 Gbps, and 100 Gbps as your requirements change, but also allows you to verify multi-speed network devices using a single lab testbed.

It is possible to setup a single lab test-bed for verifying network devices with configurable port interface speeds of 4 x 10 Gbps or 1 x 40 Gbps, by using SR4 parallel optics based transceivers and MPO/MTP cabling.

Existing product offerings from Cisco, Juniper, and several other vendors provide multi-speed configurable network devices based on supporting SR4 parallel optics in either CFP or QSFP+ form factor. A unified 10 Gbps and 40 Gbps testbed is shown in Figure 12.

Figure 12: Unified 10 and 40 Gbps testbed using SR4 optics in CFP or QSFP form factor
This unified testbed can be used for verifying both 10 Gbps and 40 Gbps modes of operation without having to change the physical testbed setup, since both the DUT and the Xena tester are configurable for either 4 x 10 Gbps or 1 x 40 Gbps modes of operation per optical transceiver cage (CFP or QSFP+ form factor).

Next generation switch silicon and network devices entering the market in 2012 will support multi-speed port configurations, where one CXP interface can be configured as either 1 x 100 Gbps, 3 x 40 Gbps, or 12 x 10 Gbps. For these 100G enabled devices, it will also be possible to setup a testbed which can support any mix of speeds using a single unified testbed setup.

In addition to the advantage of using a single physical testbed to test both 10 Gbps, 40 Gbps, and 100 Gbps modes of operation of the DUT, the unique 10/40/100G tri-speed capability of the Xena testers will also reduce the need for extra investments in test equipment to cover the different speed modes, and result in a more compact and less space demanding lab testbed installations.

**Live demo**

It’s easy to try our solutions live right now - all you need is a PC running Windows XP or later! Here’s what you do, goto [http://xenanetworks.com/html/live_demo.html](http://xenanetworks.com/html/live_demo.html)