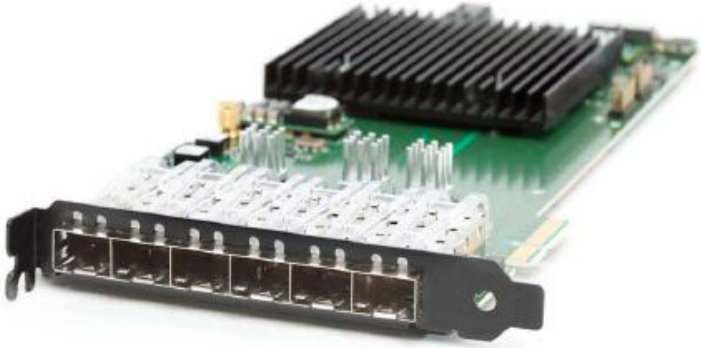
Overview

This document compares Ixia's 32-port **Xdensity 10GE** module, the 32-port **Spirent DX 10GE** module and the 6-port **M6-SFP+**test module from Xena.

Ixia Xdensity 10GE Load Module

Spirent DX 10GE



Xena Networks' M6-SFP+ (6-port 10G test module)

CONCLUSION:
Xena's test module compares favorably against both Ixia and Spirent's products. Xena has a roadmap for developing a number of features and functions that will further improve the M6-SFP+'s competitiveness.

In terms of value for money and ease of use, Xena's products offers clear advantages. Free software, free technical support, free warranty and 3 years' free software upgrades makes Xena's product easy to afford, and the user-friendly XenaManager makes it simple to quickly set-up and execute even complex test programs.

1. Modern Design Architecture and Components

Xena's solutions are based on an architecture and components that are more up to date than Ixia and Spirent which were designed more than a decade ago. In addition to port density and lower power consumption this results in some small, yet significant, advantages.

- For example, Ixia uses 4 separate Spartan II FPGAs along the transmit path from the packet scheduling to the frontend interfacing the PHY. These chips run at different clock speeds which need async FIFOs to handled data transmission, back pressure, and so on. Xena, on the other hand, has all its logic on the same FPGA where everything runs at 125 MHZ. As a result Ixia **rate control** has a hard time struggles to compete with the rate control offered by Xena.

- The same is true **of timestamp accuracy**. Xena offers a 8 ns timestamp insertion for the 125MHZ clock. Ixia runs it's timestamp clock at 50MHZ, achieving a 20ns resolution with +/- 20 ns precision.

- Xena offers a **port group inline mode**. This lets you use the Xena tester as a 1GE/10GE inline sniffer between two DUTS to capture sessions between them. This is great feature for testing vendor interoperability which would otherwise require a SPAN port or inline sniffer device.

2. User-friendly GUI

Xena's software is very easy to use. Installing the software is much easier and this positive experience is repeated in numerous areas of the GUI. Here are some examples:

- Xena's GUI makes **error injection** easier than Ixia and Spirent where you have to go to separate pages / tabs.

- **TID usability** design fits right in the middle of IxExplorer and IxNetwork.

- Xena's implementation **burst size configuration** is more intuitive and graphical than Ixia's.

- Xena's **histogram function** which includes IFG, Packet Length, and Latency is easier to use than Ixia's Latency bin design. (In fact a lot of Ixia customers probably don't even know the existence of this feature due to the non-intuitive GUI.)

- Xena lets you **export a port configuration file as an editable txt file format**, whereas Ixia uses a script generation API. Most hard core script/automation engineers really appreciate the simplicity and flexibility.

Ixia Xdensity / Spirent DX versus Xena

FEATURE	Ixia Xdensity 10GE Load Module	Spirent DX 10GE	Xena 10G test ports	COMMENTS
Load module P/N	DX-10G-S32	XDM10G32	M6SFP+	
Number of ports per load module	32-ports of SFP+	32-ports of SFP+	6-ports of SFP+	
Chassis slots per module	1	1	1	
Maximum ports per chassis: • **Large chassis** • **Small chassis**	• 12U Chassis: 384-ports • 3U Chassis: 64-ports	• 9U Chassis 192-ports • 2U Chassis 32-ports	• 4U Chassis 72-ports • 1U Chassis: 6-ports	
SFP+ transceiver support	10GBASE-SR 10GBASE-SW 10GBASE-LR 10GBASE-LW DAC (SFP+ Direct Attach)	10GBASE-SR 10GBASE-SW 10GBASE-LR 10GBASE-LW DAC (SFP+ Direct Attach)	10GBASE-SR 10GBASE-SW 10GBASE-LR 10GBASE-LW DAC (SFP+ Direct Attach)	
Interface protocols	IEEE8002.3ae10GE LAN	IEEE8002.3ae10GE LAN	IEEE8002.3ae10GE LAN	

Data center protocols	FCoE Priority-based Flow Control DCBX/LLDP, FIP, FCF	FCoE Priority-based Flow Control	No	Priority-based Flow Control on Xena roadmap
Host protocol emulation support	ARP, NDP, IPv4, IPv6, IGMP, MLD and DHCPv4/v6 The combined protocol session count is limited to 10 sessions per port regardless of protocol selection	ARP, NDP, IPv4, IPv6, IGMP, MLD and DHCPv4/v6 10 sessions per protocol per port	ARP	NDP on Xena roadmap
Performance benchmark tests	RFC 2544 RFC 2889	RFC 2544 RFC 2889 RFC 3918	RFC 2544 RFC 2889	
Per port reservation	No (8 ports per user)	No (4 ports per user)	Yes (per port)	
Stream definitions per port	16	4096	256	
Transmit engine	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures	Wire-speed packet generation with timestamps, sequence numbers, data integrity signature, and packet group signatures	
Field Modifiers per stream	5	4	5	
Frame length controls	Increment, Decrement, Random per individual stream (16)	Increment, Decrement, IMIX and Random Only one mode at a time for ALL Streamblocks	Increment, Decrement, IMIX and Random per individual stream (256)	

Error generation	CRC error, undersize length, oversize length	CRC error, undersize length, oversize length(60 B min, 16004 max)	CRC error, payload error, test payload error, sequence error, misorder error, undersize length (56B min) and oversize length (16384 max)	
Checksum generation in hardware	IPv4, UDP, TCP, ICMP, ICMPv6, IGMP	IPv4, UDP, TCP	IPv4, UDP	
Trackable receive flows	8K per port	4k	2K	
Filters	2x128-bit user-definable patterns	No	Number of filters: 6 - 6 x 64-bit user-definable match-term patterns with mask, and offset - 6 frame length comparator terms (longer, shorter) - 6 user-defined filters expressed from AND/OR'ing of the match and length terms.	

Statistics and rates (counter size: 64 bits)	Link state, line speed, frames sent, valid frames received, bytes sent/received, fragments, undersize, oversize, CRC errors, VLAN tagged frames, 6 user-defined stats (UDS), data integrity frames, data integrity errors, sequence checking frames, sequence checking errors, ARP, and ping requests and replies	Link state, line speed, frames sent, valid frames received, bytes sent/received, fragments, undersize, oversize, CRC errors, ARP, and ping requests and replies	Link state, line speed, frames sent, valid frames received, bytes sent/received, CRC errors, 6 user-defined stats (UDS), data integrity frames, data integrity errors, sequence checking frames, sequence checking errors, ARP, and ping requests and replies	
Flow Control	IEEE802.3x PAUSE frame control IEEE802.1Qbb(PFC)	IEEE802.3x PAUSE frame control IEEE802.1Qbb(PFC)	IEEE802.3x PAUSE frame control	IEEE802.1Qbb(PFC) on roadmap
Latency measurements	Hardware-based latency measurements supporting: Store & Forward latency Cut-Through latency 20 ns resolution in packet timestamp	No	Hardware-based latency measurements supporting: Store & Forward latency Cut-Through latency 8 ns resolution in packet timestamp	
Jitter measurement	No	No	Yes (MEF10 compliant)	July 2012 release
Timing sync of chassis	Yes	n/a	No	On Xena roadmap

Transmit line clock adjustment	-100 to +100 ppm	-100 to +100 ppm	-400 to +400 ppm	July 2012 release
Bandwidth profiles	Interleaved uniform and bursty, stop after N packets Sequential scheduling (weak packet interleaving accuracy, weak burst specification)	Uniform	Interleaved uniform and bursty, stop after N packets Sequential scheduling very accurate packet spacing and scheduling	
Capture functionality	No	Yes, can capture first 80 byte per packet	Yes, 64kB wire-speed buffer. Capture triggers (filters, errors), before/after Capture limit per packet Wireshark “hotbutton”	
Histograms per port	None	None	2 (select independently IFG / Latency / Packet length per histogram)	
Scripting support	Subset	Yes	Full feature set via generic CLI for Tcl, Perl, Python, Java, VBA, C, C#	
Port loopmodes	Rx-2-tx L2 Rx-2-tx L3	Rx-2-tx L2 Rx-2-tx L3	Rx-2-tx L2 Rx-2-tx L3 Port-2-Port (inline) with analysis capability	